HIGH SPEED POWER DRIVER

Check for Samples: UC1705, UC2705, UC3705

FEATURES

- **1.5 A Source/Sink Drive**
- **100 nsec Delay**
- **40 nsec Rise Fall into 1000 pF**
- **Inverting and Non-Inverting Inputs**
- **Low Cross-Conduction Current Spike**
- **Low Quiescent Current**
- **5 V to 40 V Operation**
- **Thermal Shutdown Protection**
- **Minidip and Power Packages**

DESCRIPTION

The UC1705 family of power drivers is made with a high sppeed Schottky process to interface between low-level control functions and high-power switching devices - particularly power MOSFETs. These devices are also an optimum choise for capacitive line drivers where up to 1.5 A may be switched in either direction. With both inverting and non-inverting inputs available, logic signals of either polarity may be accepted, or one input can be used to gate or strobe the other.

Supply voltages for both V_S and V_C can independently range from 5 V to 40 V. For additional application details, see the UC1707/3707 data sheet (SLUS177).

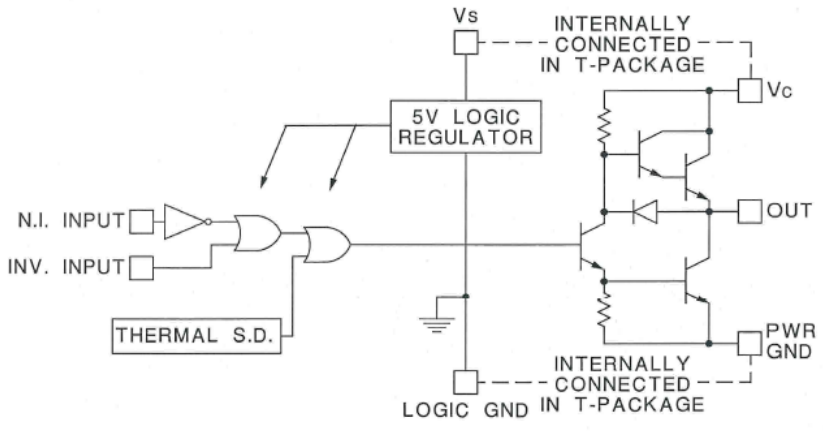
The UC1705 is packaged in an 8-pin hermetically sealed CERDIP for -55°C to 125°C operation. The UC3705 is specified for a temperature range of 0°C to 70°C and is available in either a plastic minidip or a 5-pin, power TO-220 package.

TRUTH TABLE (1) (2)

INV	N.I	OUT
H	H	L
L	H	H
H	L	L
L	L	L

(1) $\overline{OUT}$ = $\overline{INV}$ and N.I.
(2) $\overline{OUT}$ = INV and N.i.

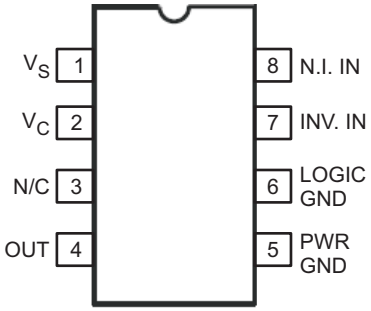
BLOCK DIAGRAM



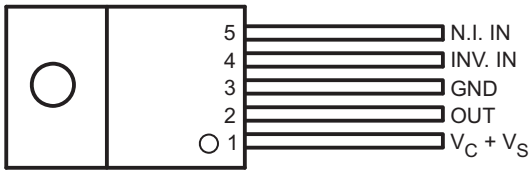
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

CONNECTION DIAGRAMS

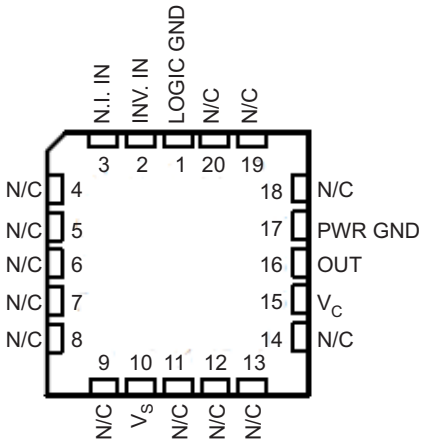
DIL-8 MINIDIP, SOIC-8
(TOP VIEW)
N, JG OR D PACKAGE



5-PIN TO-220
(TOP VIEW)
T PACKAGE



LCCC-20
(TOP VIEW)
FK PACKAGE



ABSOLUTE MAXIMUM RATINGS(1)

	VALUE			UNIT
	N-Pkg	JG-Pkg	T-Pkg	
Supply Voltage (V_{IN})	40	40	40	V
Collector Supply Voltage, V_C	40	40	40	
Output current (source or sink)				
Steady-State	±500	±500	±1	A
Peak Transient	±1.5	±1	±2	A
Capacitive Discharge Energy	20	15	50	µJ
Digital Inputs (2)	5.5	5.5	5.5	V
Power Dissipation at T_A = 25°C (1)	1	1	3	W
Power Dissipation at T_A (Lead/Case) = 25°C (1)	3	2	25	W
Operating Temperature Range	0 to 70	–55 to 125	0 to 70	°C
Storage temperaturee	–65 to 150	–65 to 150	–65 to 150	°C

(1) All currents are positive into, negative out of the specified terminal.
(2) Digital Drive can exceed 5.5 V if the input current is limited to 10 mA

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications apply for T_A = –55°C to +125°C for the UC1705, –25°C to +85°C for the UC2707, and 0°C to +70°C for the UC3705; $V_{IN} = V_C$ = 20 V. $T_A = T_J$.

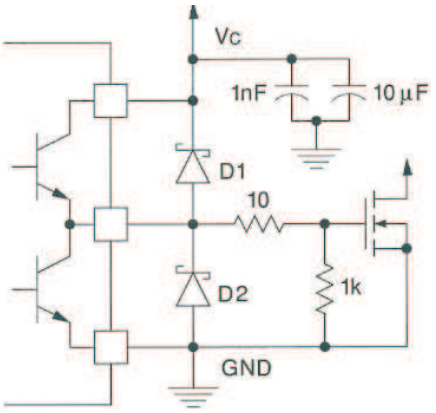
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_S	Supply current	V_S = 40 V, outputs high, T package		6	8	mA
		V_C = 40 V, outputs low, T package		6	12	mA
V_C	Supply current (N, JG Only)	V_C = 40 V, outputs low		2	4	mA
V_C	Leakage current (N, JG Only)	V_S = 0, V_C = 30 V		0.05	0.1	mA
	Digital input low level				0.8	V
	Digital input high level		2.2			V
	Input current	V_I = 0		–0.6	–1	mA
	Input leakage	V_I = 5 V		0.05	0.1	mA
$V_C – V_O$	Output high saturation	I_O = –50 mA			2	V
		I_O = –500 mA			2.5	
V_O	Output low saturation	I_O = –50 mA			0.4	V
		I_O = –500 mA			2.5	
	Thermal shutdown			155		°C

TYPICAL SWITCHING CHARACTERISTICS

V_{IN} = V_C = 20 V, T_A = 25°C. Delays measured to 10% output change.

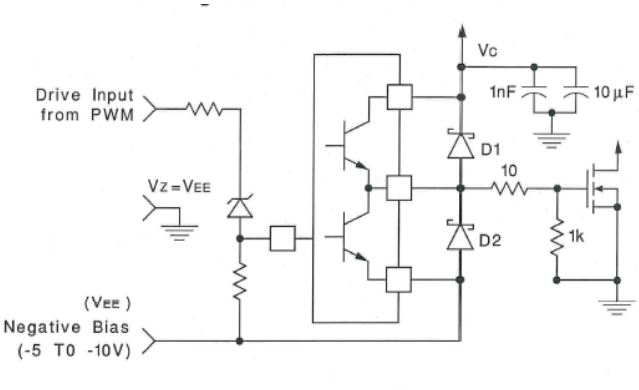
PARAMETER	TEST CONDITIONS	OUTPUT CL =			UNIT
From Inv. Input to Output		open	1	2.2	nF
Rise time delay		60	60	60	ns
10% to 90% rise		20	40	60	ns
Fall time delay		60	60	60	ns
90% to 10% fall		25	40	50	ns
From N.I. Input to Output					
Rise time delay		90	90	90	ns
10% to 90% rise		20	40	60	ns
Fall time delay		60	60	60	ns
90% to 10% fall		25	40	50	ns
V_C cross-conduction current spike duration	Output rise	25			ns
	Output fall	0			ns

APPLICATION INFORMATION



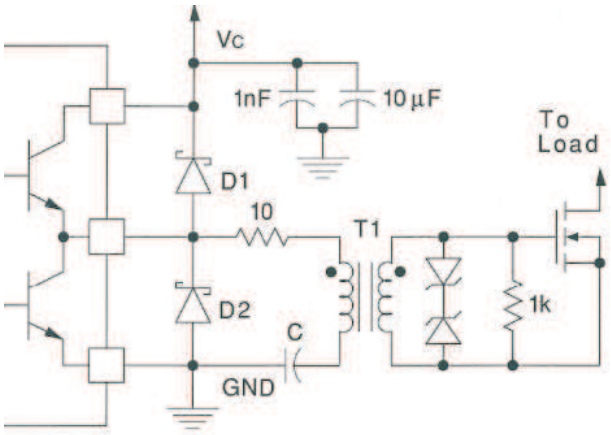
D1, D2: UC3611 Schottky Diodes

Figure 1. Power MOSFET Drive Circuit



D1, D2: UC3611 Schottky Diodes

Figure 2. Power MOSFET Drive Circuit Using Negative Bias Voltage and Level Shifting to Ground Referenced PWMs



D1, D2: UC3611 Schottky Diodes

Figure 3. Transformer Coupled MOSFET DRIVE Circuit

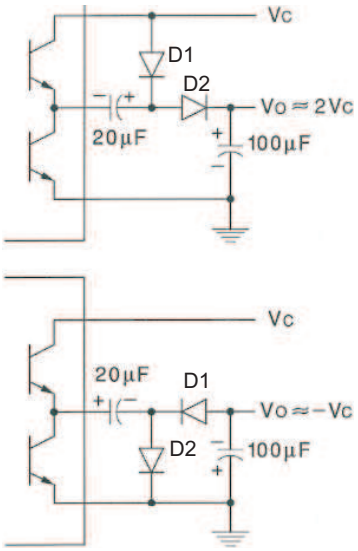


Figure 4. Charge Pump Circuit

REVISION HISTORY

Changes from Revision C (December, 2011) to Revision D	Page
• Deleted SN54BCT373 from title for FK package image	2

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
5962-9579801M2A	ACTIVE	LCCC	FK	20	1	TBD	Call TI	Call TI	
5962-9579801MPA	ACTIVE	CDIP	JG	8	1	TBD	Call TI	Call TI	
5962-9579801VPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
UC1705J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
UC1705J883B	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
UC1705L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	
UC2705D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UC2705DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UC2705N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC2705NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC3705D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UC3705DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UC3705DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UC3705DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
UC3705J	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	
UC3705N	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC3705NG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	
UC3705T	ACTIVE	TO-220	KC	5	50	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	
UC3705TG3	ACTIVE	TO-220	KC	5	50	Green (RoHS & no Sb/Br)	CU SN	N / A for Pkg Type	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

OTHER QUALIFIED VERSIONS OF UC1705, UC1705-SP, UC3705, UC3705M :

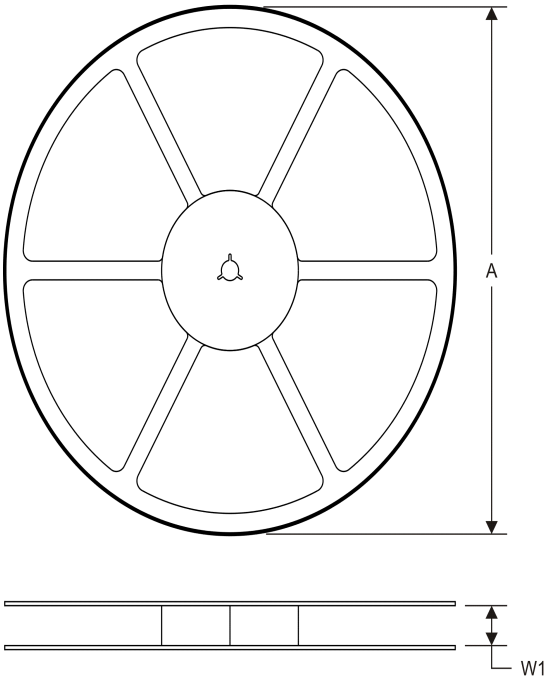
- Catalog: UC3705, UC1705, UC3705M, UC3705
- Military: UC1705
- Space: UC1705-SP

NOTE: Qualified Version Definitions:

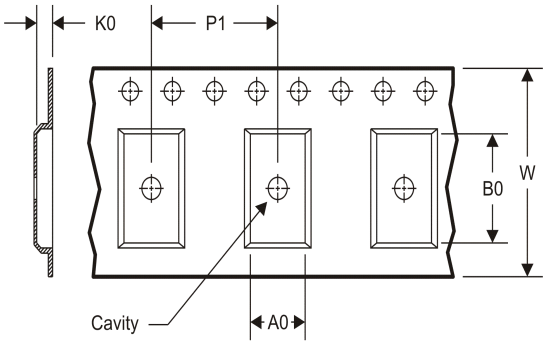
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



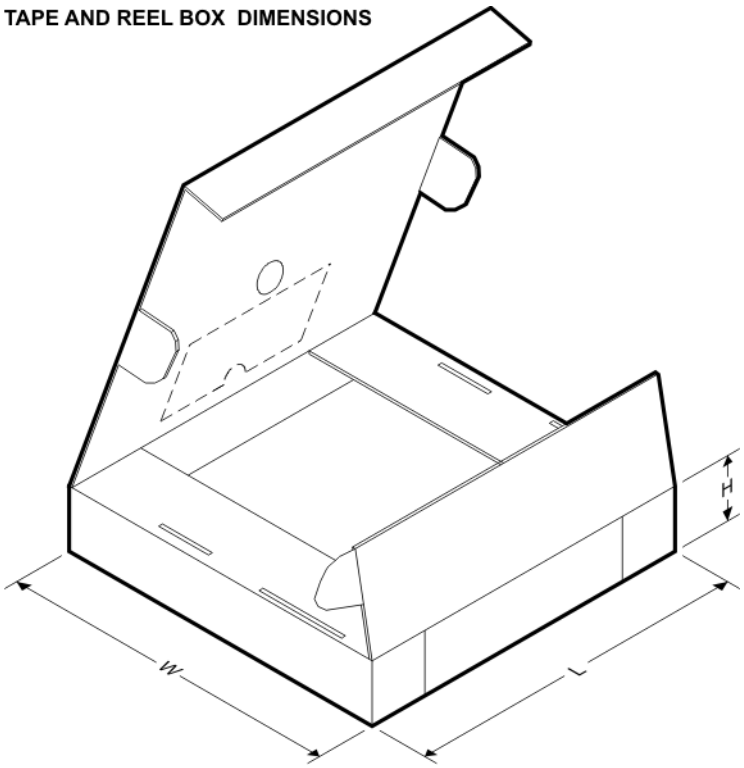
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC3705DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

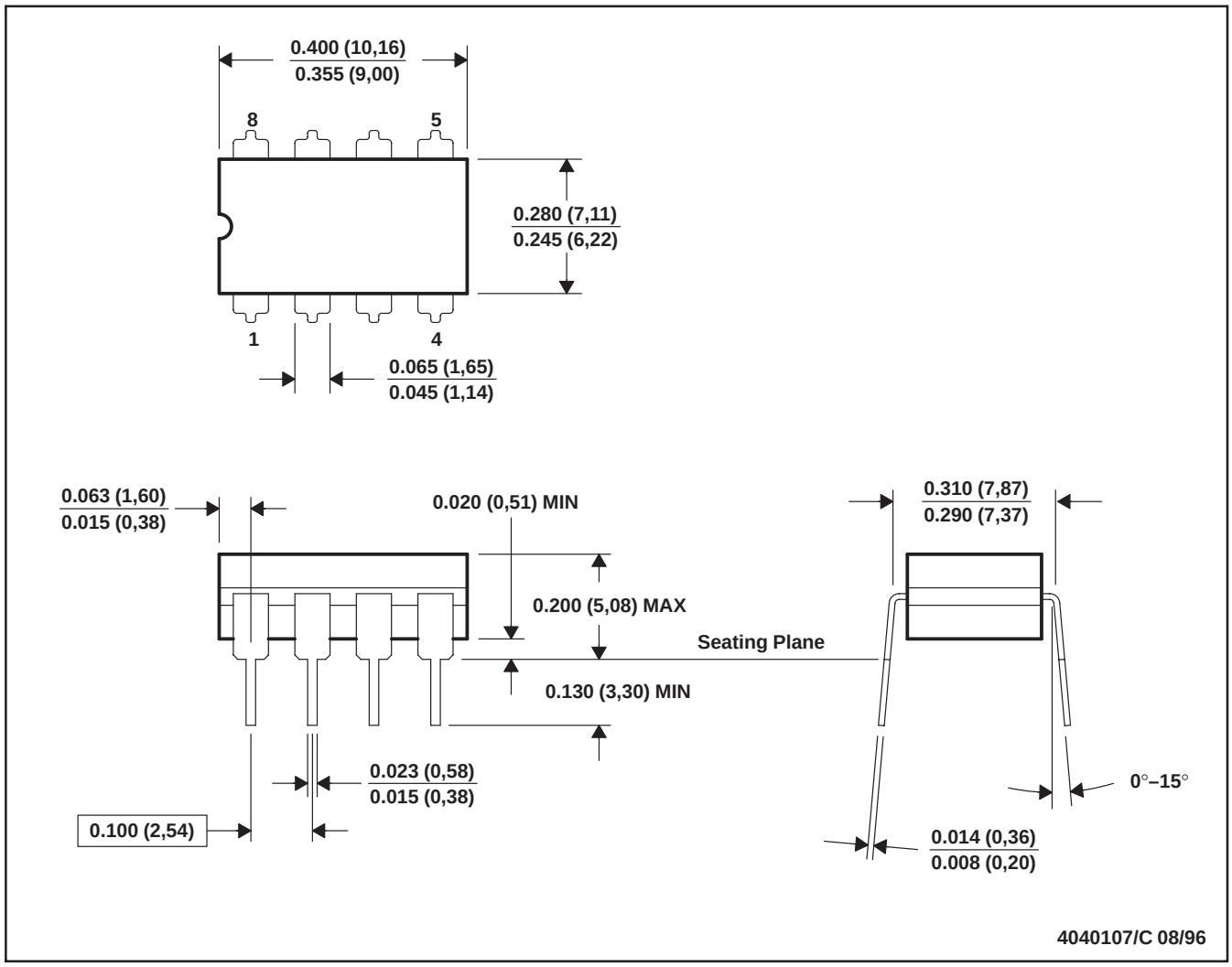


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC3705DTR	SOIC	D	8	2500	367.0	367.0	35.0

MCER001A – JANUARY 1995 – REVISED JANUARY 1997

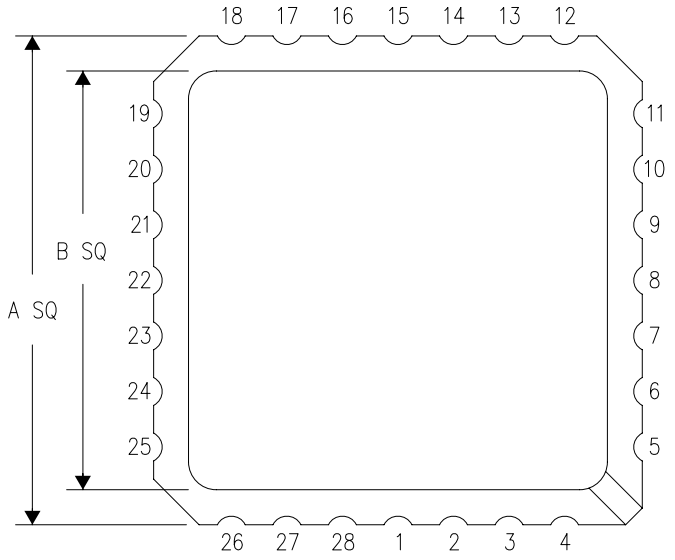
JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



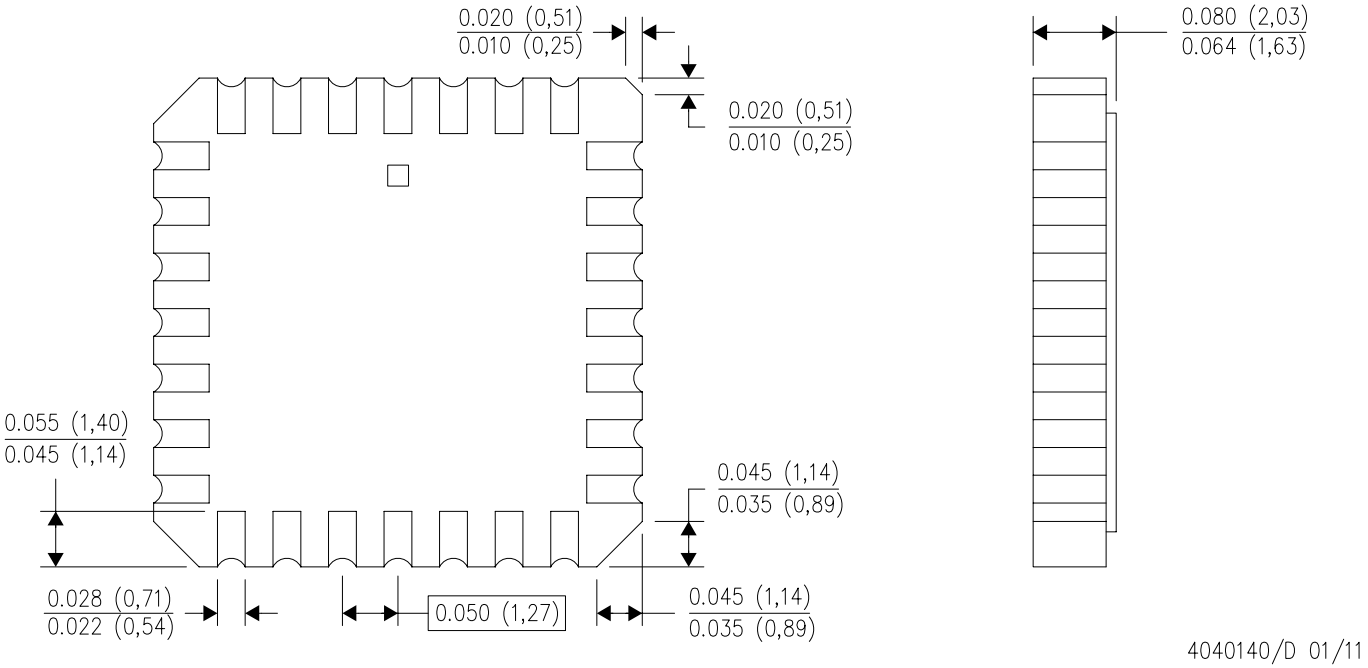
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



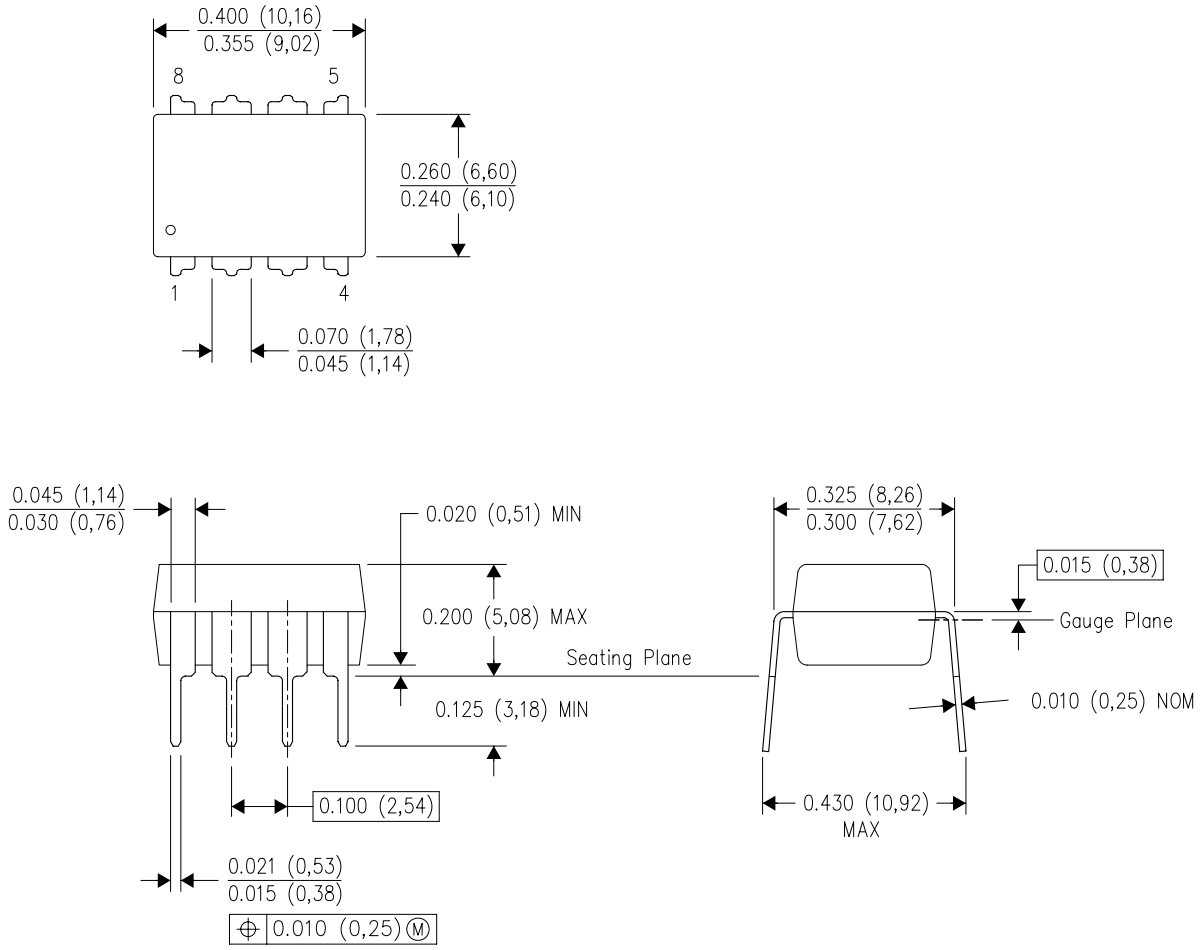
NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

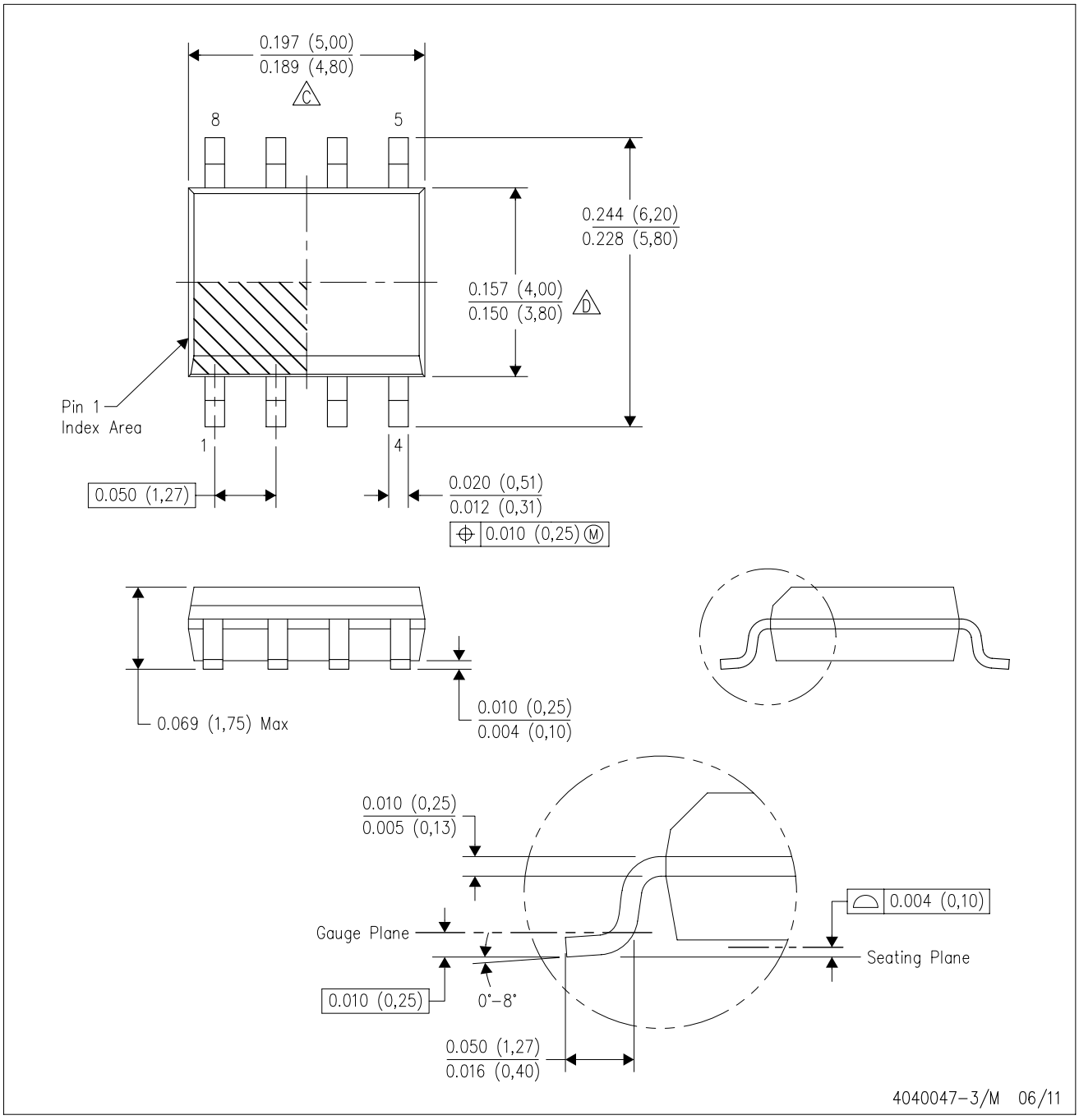
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



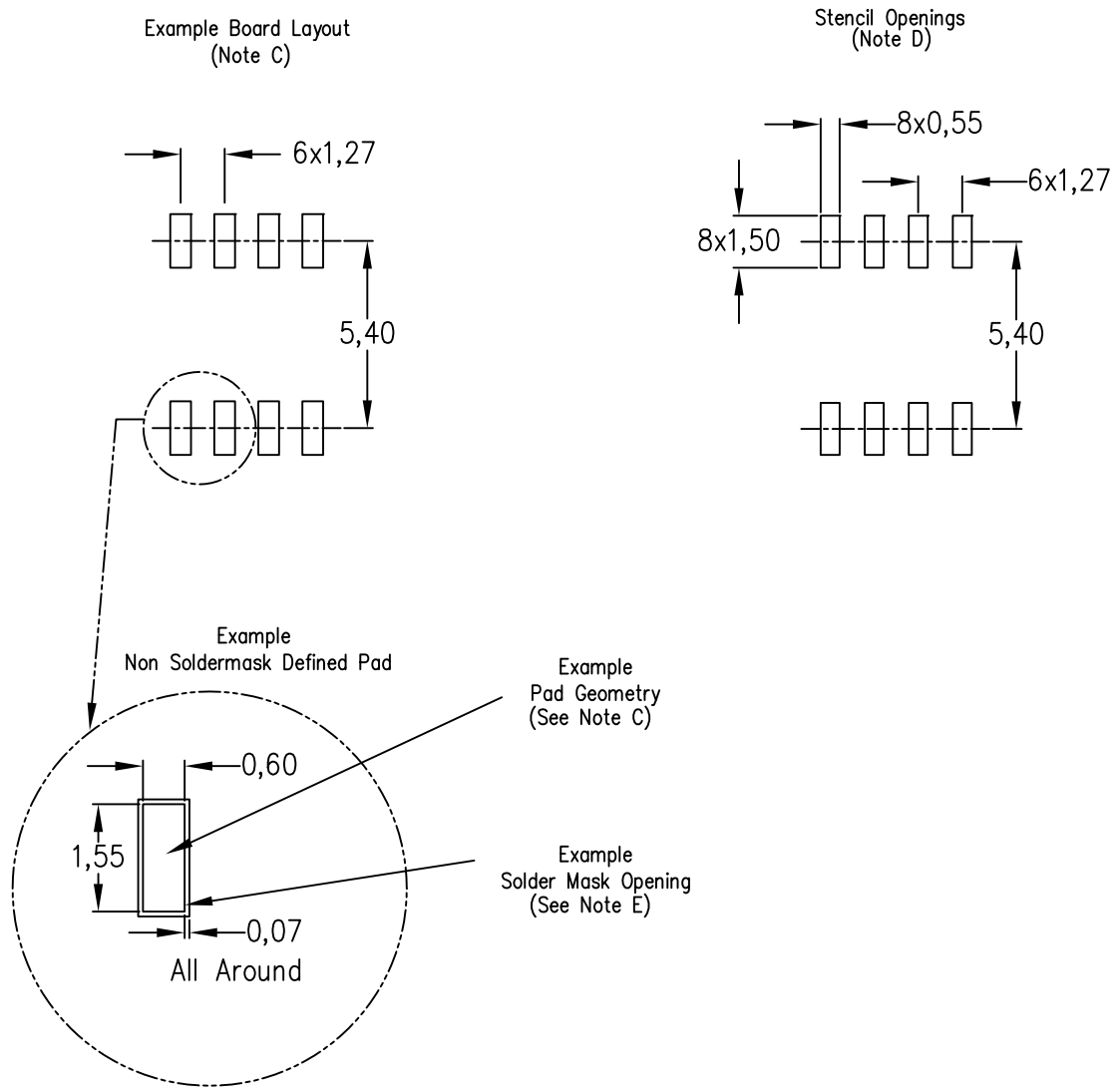
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



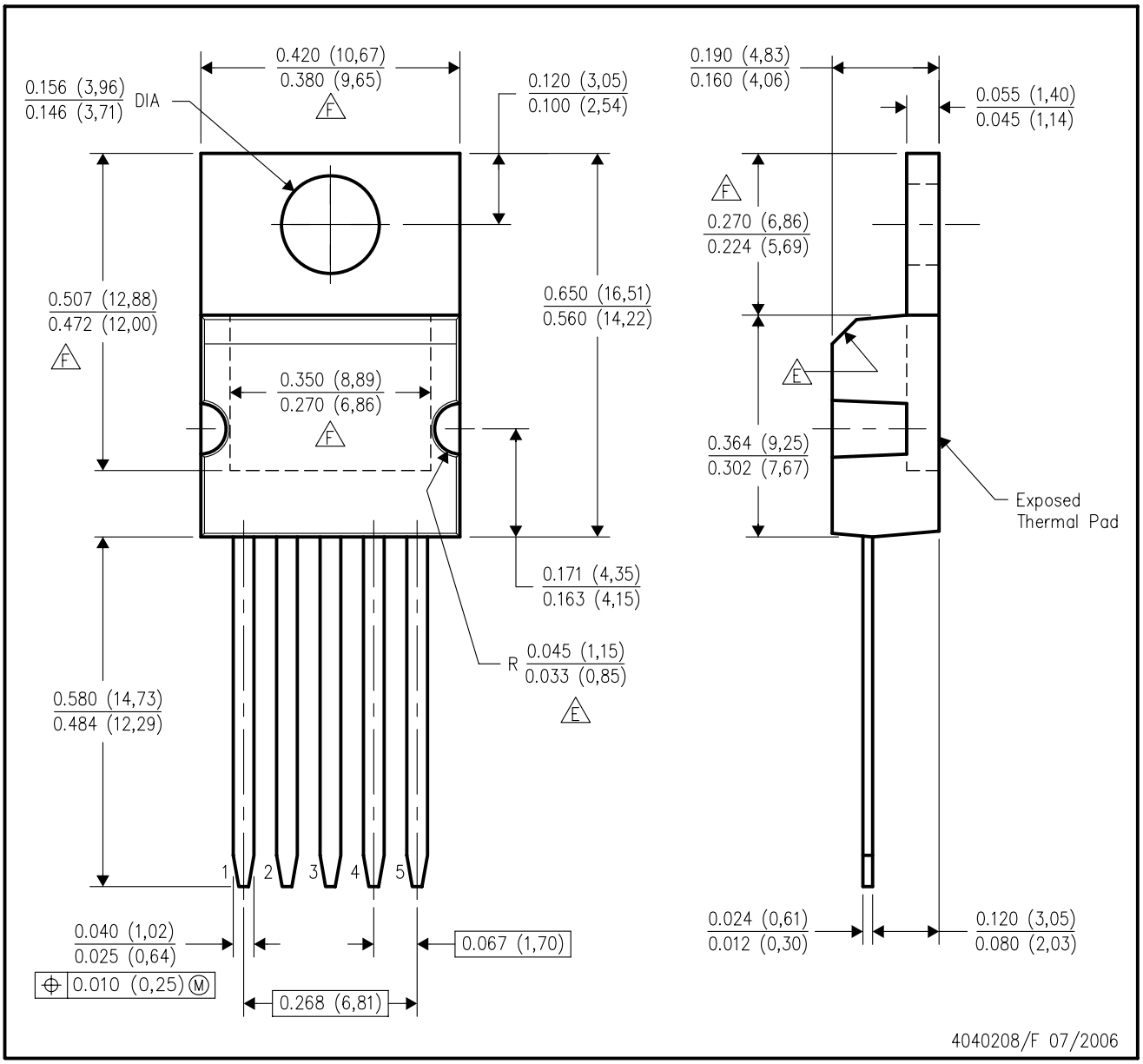
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

KC (R–PSFM–T5) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. All lead dimensions apply before solder dip.
D. The center lead is in electrical contact with the mounting tab.
E. These features are optional.
F. Thermal pad contour optional within these dimensions.

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